

FIG. 1
PRIOR-ART

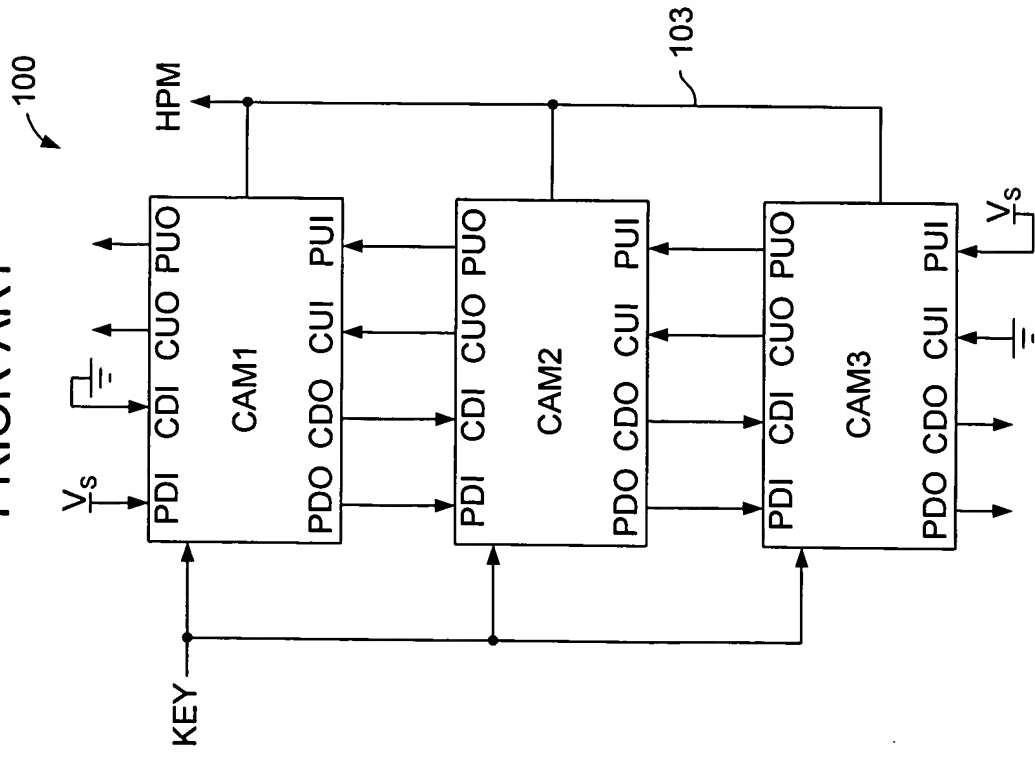
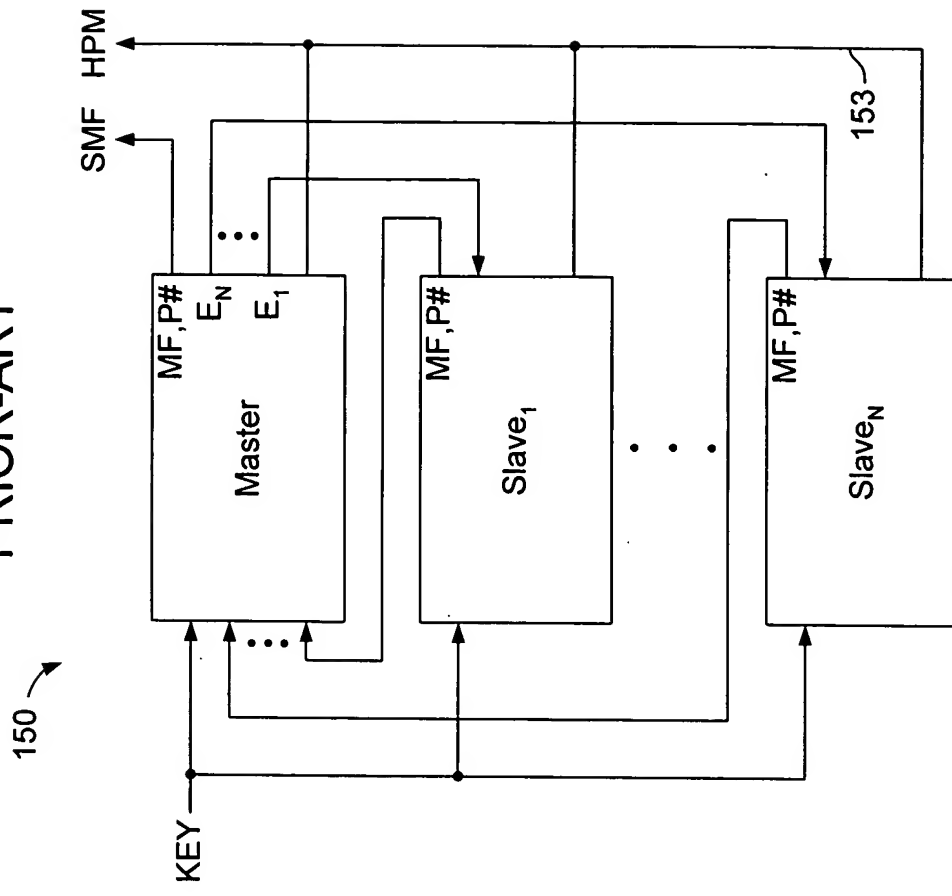


FIG. 2
PRIOR-ART



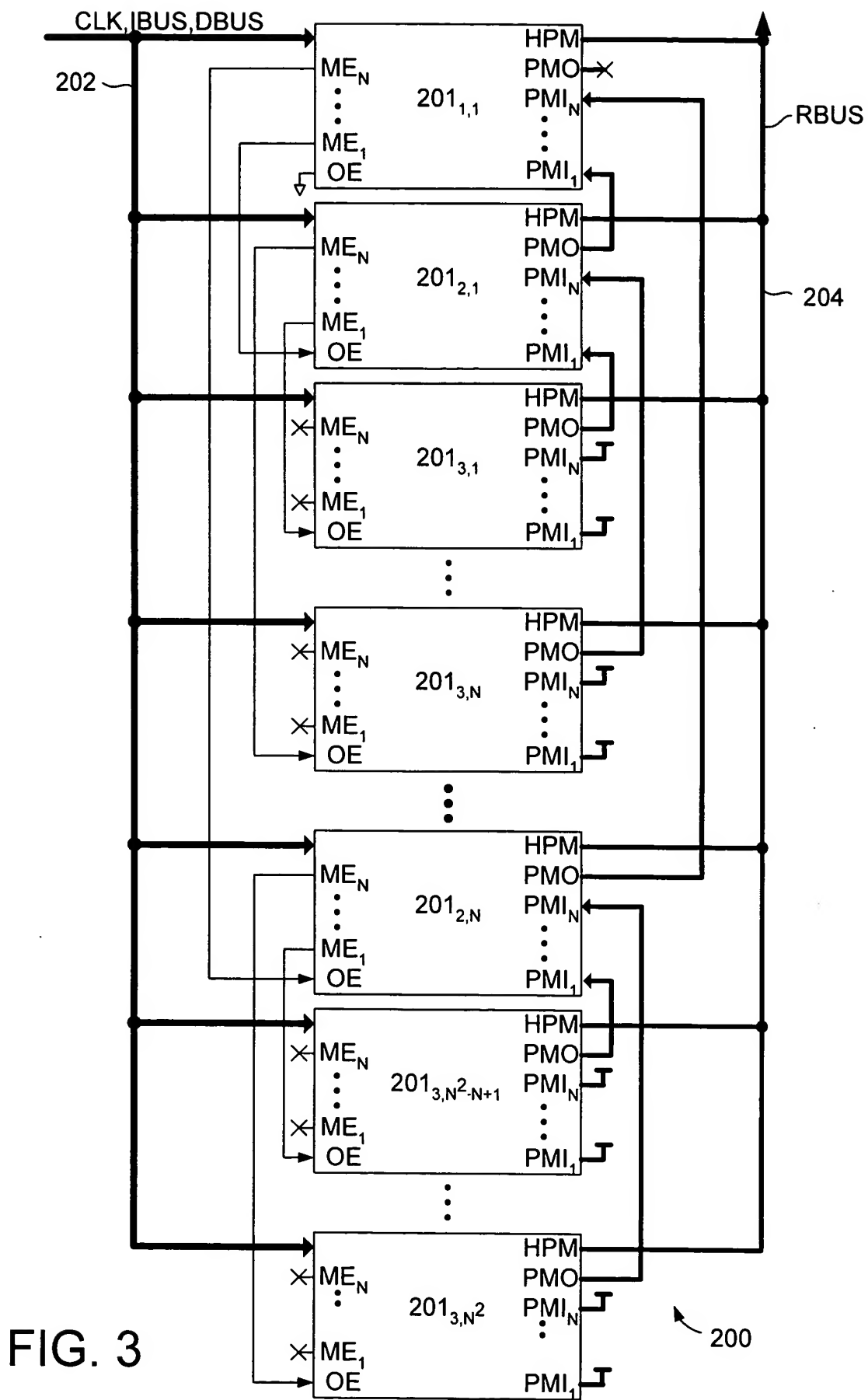
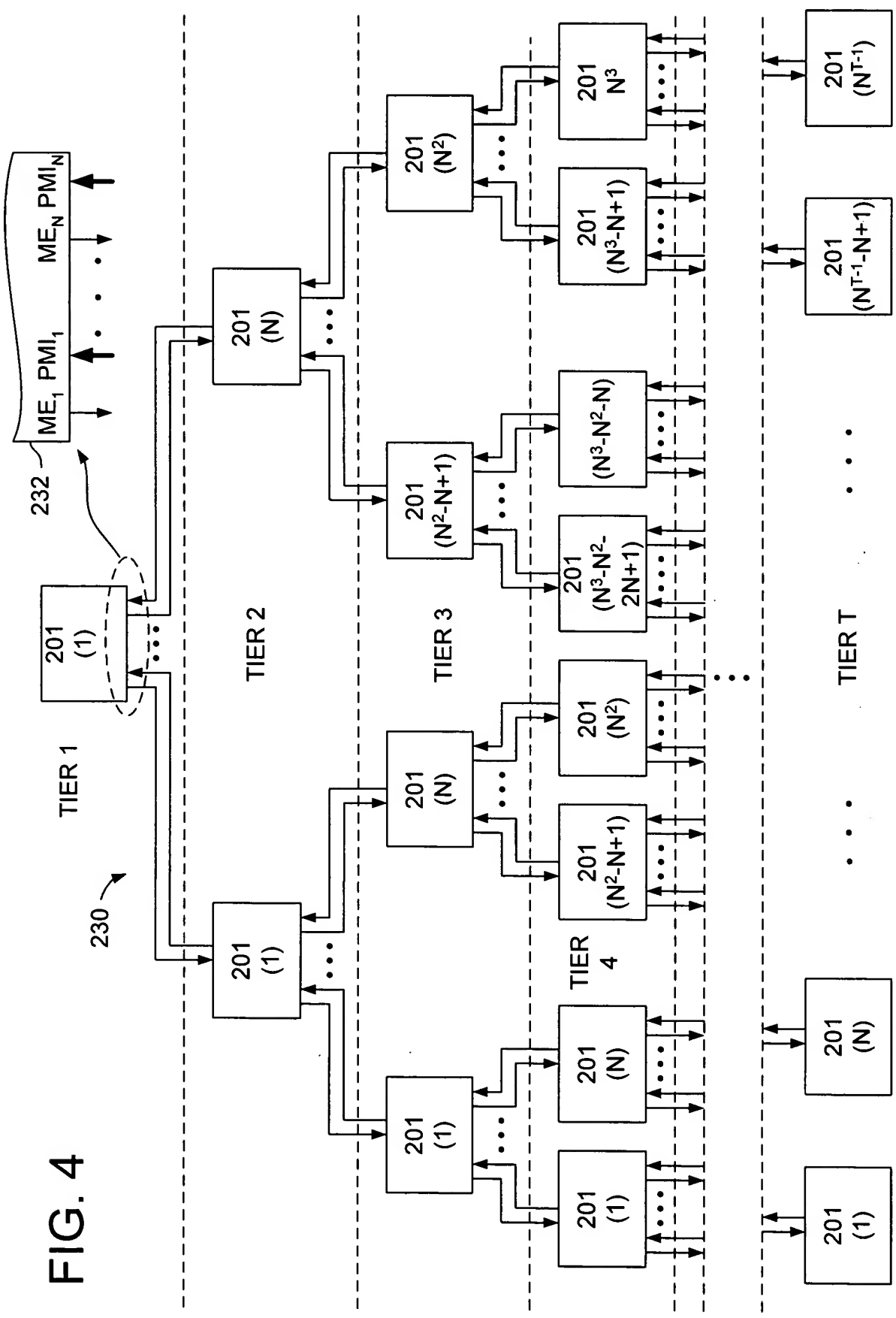


FIG. 3

FIG. 4

The diagram illustrates a multi-tier system architecture. At the top, a block labeled **201 (1)** is connected to a set of blocks labeled **232**, which includes **ME₁ PMI₁**, **ME_N PMI_N**, and intermediate blocks indicated by ellipses. Below this, the system is divided into horizontal sections by dashed lines, labeled **TIER 1**, **TIER 2**, **TIER 3**, **TIER 4**, and **TIER T**. Each tier contains one or more blocks labeled **201** with various indices. For example, **TIER 2** contains **201 (1)** and **201 (N)**. **TIER 3** contains **201 (1)**, **201 (N)**, **201 (N²-N+1)**, and **201 (N²)**. **TIER 4** contains **201 (1)**, **201 (N)**, **201 (N²-N+1)**, **201 (N²)**, **201 (N³-N²-2N+1)**, and **201 (N³-N²-N)**. **TIER T** contains **201 (1)**, **201 (N)**, **201 (N^{T-1}-N+1)**, and **201 (N^{T-1})**. Arrows indicate data flow between blocks within a tier and between tiers. A vertical ellipsis on the right side indicates that there are more tiers between TIER 4 and TIER T.



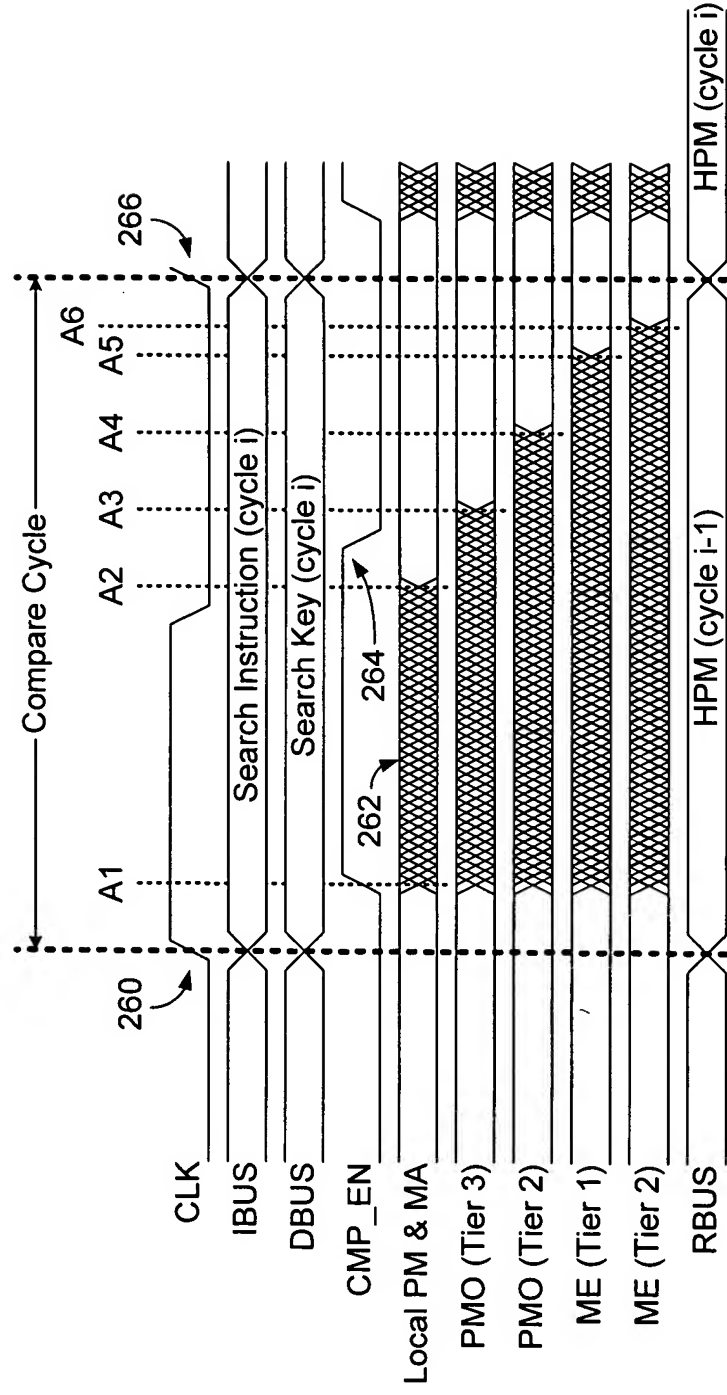
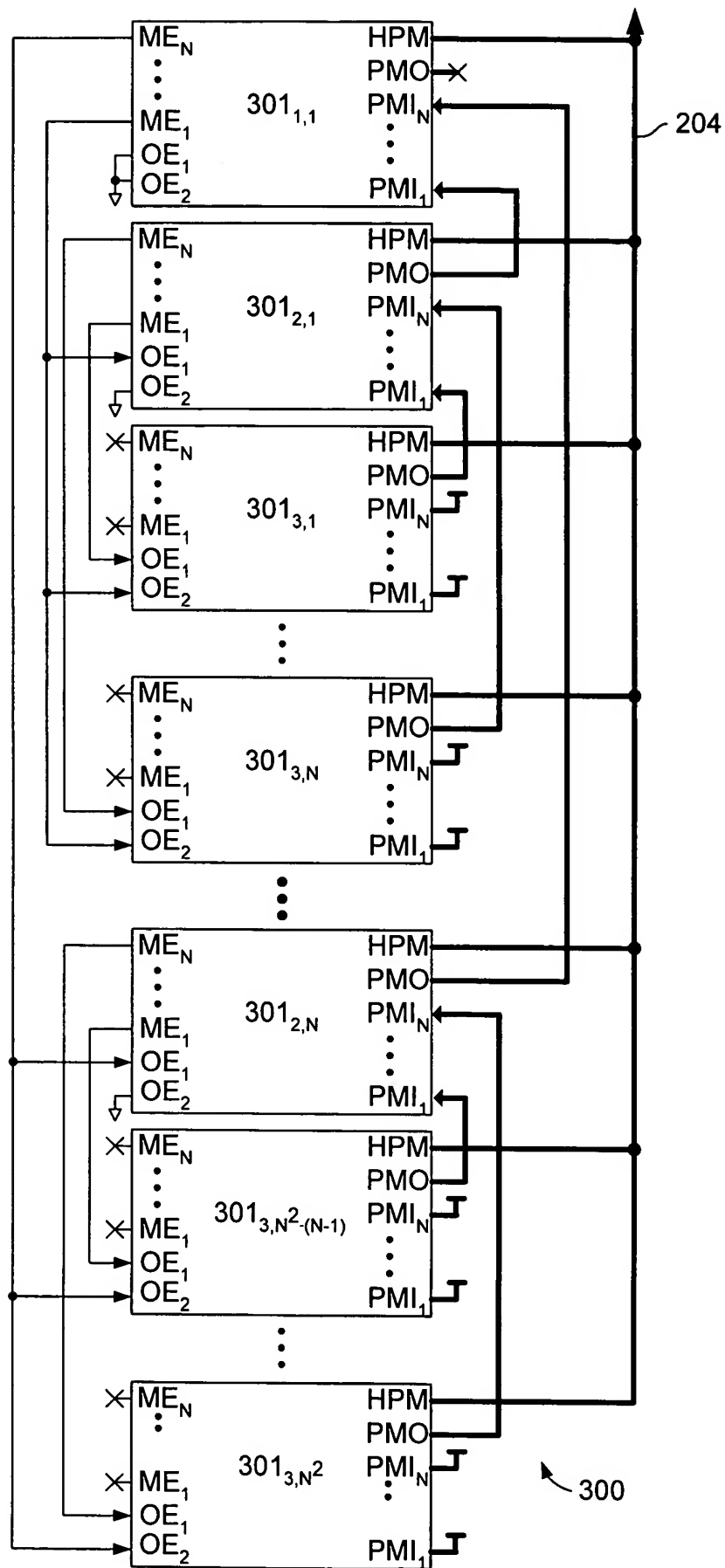


FIG. 5

FIG. 6



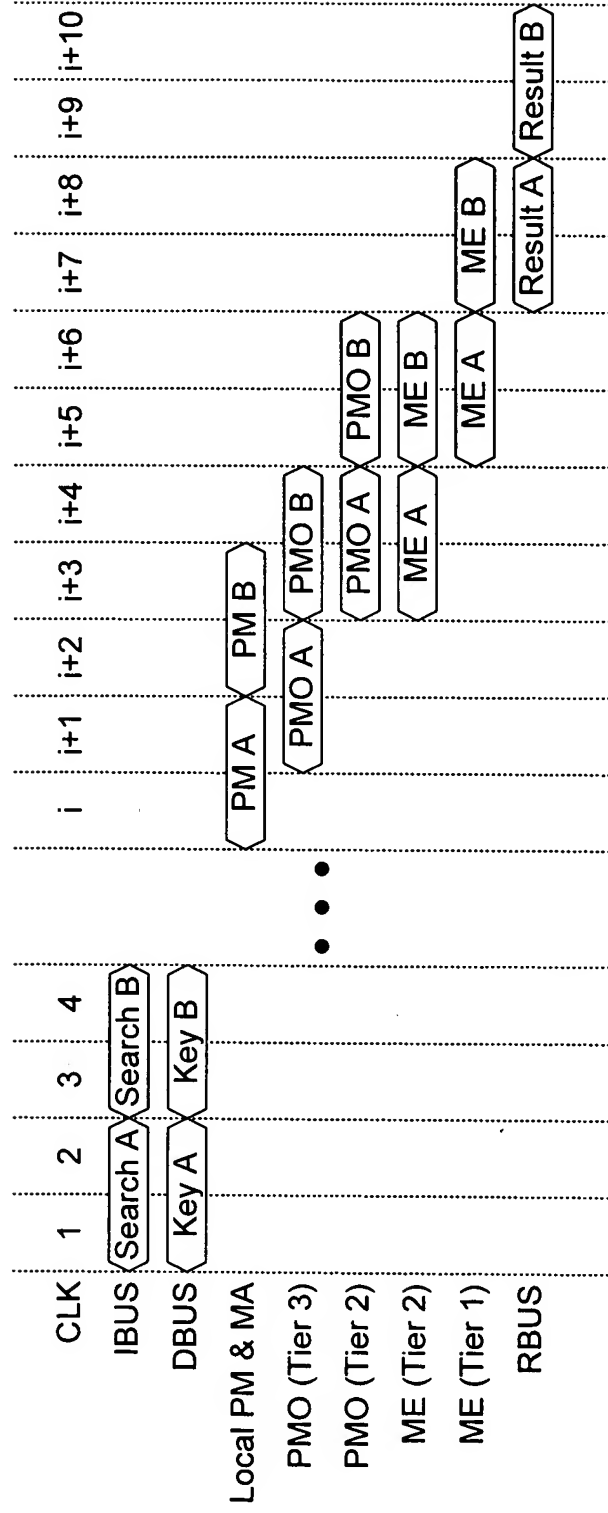


FIG. 7

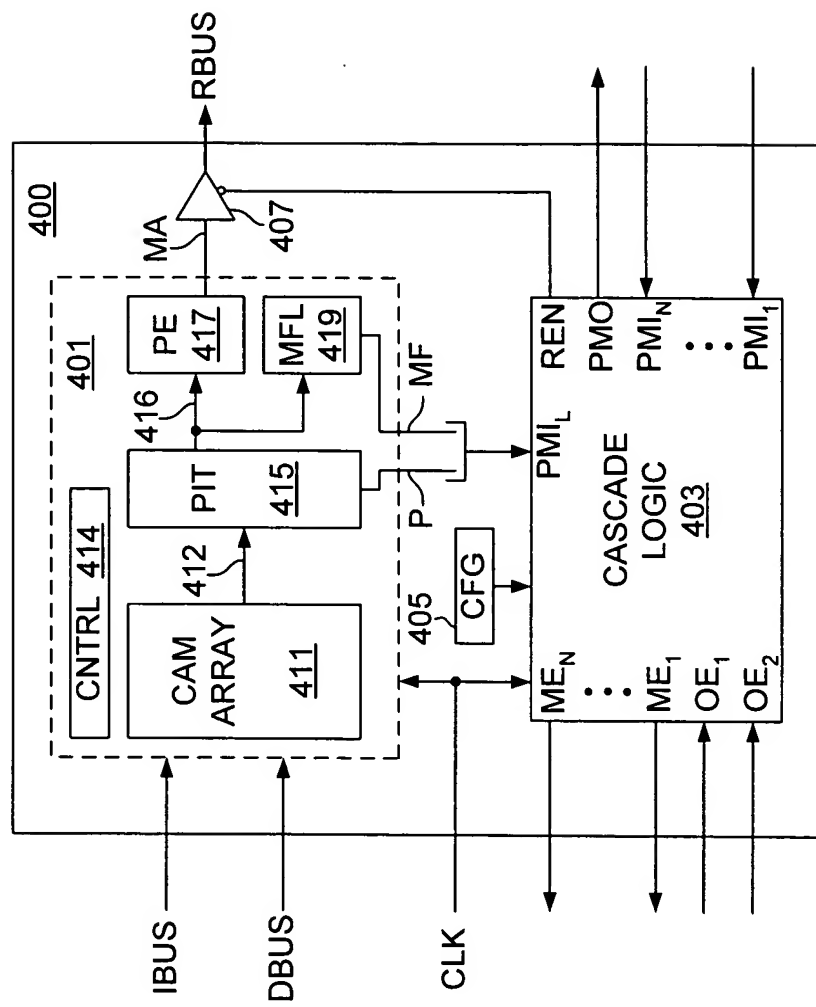


FIG. 8

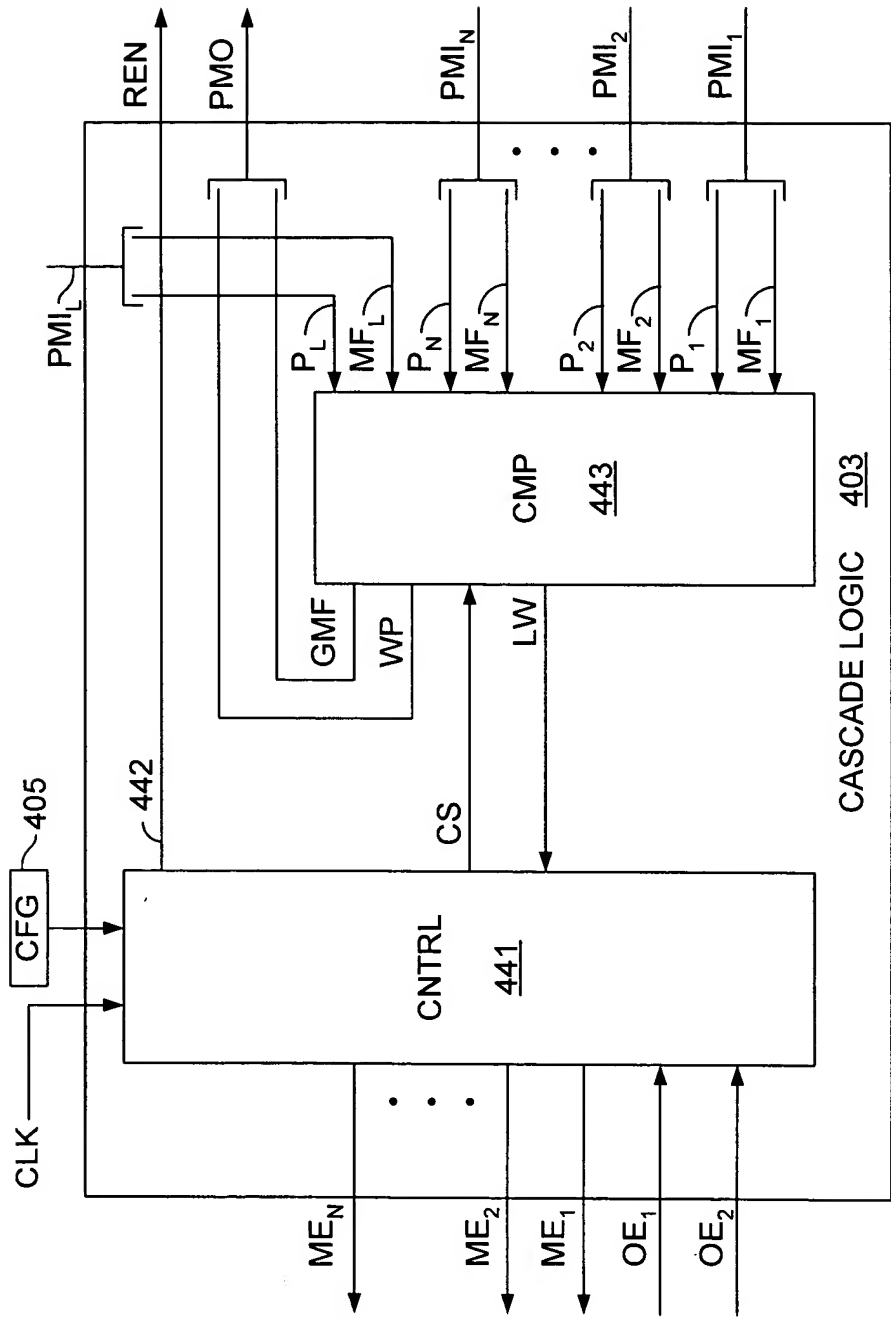


FIG. 9